a plurality of bonding pads on said wiring layer, said substrate and said first and second semiconductor chips;

a plurality of bonding wires for connecting said plural bonding pads to each other; and

a via hole in said wiring layer, said via hole having a contact for connecting one of said plural bonding pads on the wiring layer to one of said plural bonding pads on said first semiconductor chip.

--21. (new) The semiconductor device according to claim 20, further comprising a connection wire for connecting said one of said plural bonding pads on the wiring layer to another one of said plural bonding pads on said wiring layer.--

Please charge the fee of $84 for the one extra independent claim added herewith, to Deposit Account No. 25-0120.

REMARKS

A proposed drawing correction is submitted herewith for Figures 5 and 6.

The specification has been amended to make editorial changes therein to place the application in condition for allowance at the time of the next Official Action.

Claims 1-3 and 5 are rejected as being anticipated by TAKIAR et al. 5,502,289 and claims 4 and 6 are rejected as being unpatentable over TAKIAR et al. in view of TOKUDA et al. 5,870,289.

Reconsideration and withdrawal of the rejections are respectfully requested because the references neither disclose nor suggest a wiring layer between first and second semiconductor chips, the wiring layer including a polyimide tape having a copper foil layer therein as recited in new independent claims 7 and 20; nor do the references teach or suggest a wiring layer between the first and second semiconductor chips, the wiring layer including a conductor within the wiring layer as recited in new independent claim 12; nor do the references teach or suggest the wiring layer between first and second semiconductor chips, the wiring layer including a conductor traversing the wiring layer as recited in new independent claim 17.

TAKIAR et al. in Figure 7, for example, show first and second semiconductor chips 136 and 140. Substrate material 138 is between the semiconductor chips. Column 4, lines 50-63, of TAKIAR et al. disclose that the substrate material may be ceramic, metal, silicon, or a plastic circuit board material.

TOKUDA et al. is cited for the teaching of a through-hole through a wiring layer. As seen in Figure 1, for example, of TOKUDA et al. a direct-through-hole connection 40 is through wiring substrate 20. Column 10, lines 52-57, of TOKUDA et al. teach that the wiring substrate 20 is made of a layer of a thin wiring film (having a thickness of, for example, 50 μcm). The wiring film is made of a polyimide film of polymer materials.

This polyimide film has a particularly small dielectric coefficient.

The above-noted features of claims 7, 12, 17, and 20 are missing from each of the references, are absent from the combination, and thus are not obvious to one having ordinary skill in the art.

The dependent claims also include features not disclosed in the combination of references. For example, claims 9, 13, 19, and 21 recite first and second pads on the wiring layer connected by a connection wire. This feature is not disclosed in the reference and thus these claims are believed patentable regardless of the patentability of the claims from which they depend.

Accordingly, it is believed that the new claims avoid the rejections under §102 and §103 and are allowable over the art of record.

In view of the present amendment and the foregoing remarks, it is believed that the present application has been placed in condition for allowance. Reconsideration and allowance are respectfully requested.

Attached hereto is a marked-up version showing the changes made to the specification. The attached page is captioned "VERSION WITH MARKINGS TO SHOW CHANGES MADE."

Respectfully submitted,

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"VERSION WITH MARKINGS TO SHOW CHANGES MADE"

IN THE SPECIFICATION:

Page 1, the paragraph, beginning on line 22, bridging pages 1 and 2, has been amended as follows:

--Since the bonding pad on the substrate is provided around the semiconductor chip in the lowermost layer, the upper layer semiconductor chip with a smaller chip size has a longer distance with respect to the bonding pad on the substrate. Therefore, with a larger chip size difference in the upper layer and the lower layer, the distance between the bonding pad of the upper layer semiconductor chip and the bonding pad on the substrate becomes longer. In particular, [in] the [case a] wire [per one loop] connecting the substrate to the chip becomes longer[,]. Accordingly, the wire strength is lowered so that [a trouble of] sagging of the wire by its [self] own weight[, tilting] occurs. Tilting of the wire at the time of sealing, or the like is generated so as to deteriorate the yield, [and thus it] which is problematic.--.

Page 2, the paragraph, beginning on line 22, has been amended as follows:

--Accordingly, an object of the present invention is to provide a novel semiconductor device with an improved yield by solving the problems in the above-mentioned conventional technology, in particular, by shortening the wire length per one

loop so as to eliminate the problems of wire sagging by its [self] own weight, tilting of the wire at the time of sealing, or the like.--.

Page 6, the paragraph, beginning on line 18, has been amended as follows:

--The second embodiment comprises the semiconductor device shown in FIG. [1] 2, wherein relaying pads 71a, 71b are connected electrically by a wiring 72 in the inner layer of a polyimide tape 7.--.